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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,807	01/05/2004	Shinpei Kubota	0951-0130P	1617

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EXAMINER	
FLORES, LEON	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	02/02/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 02/02/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/750,807	KUBOTA, SHINPEI	
	Examiner	Art Unit	
	Leon Flores	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/5/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 6-10 should be designated by a legend such as --***Prior Art***-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters **1-11** and **301-311** have both been used to designate an **antenna, LNA, mixer, VCO, variable gain amplifier, level detection circuit, comparing circuit, limiter amplifier, phase circuit, demodulating mixer, LPF, respectively. Furthermore, the reference character in (figures 2 and 7) and (figures 4 and 8) have both been used to designate similar components.** Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 3 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 3 recites limitations, "gain switching detection circuit", which has already been addressed in claim 1.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> **The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.**

Claims 1-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Re claim 1, the limitation "*at least one gain switching detection circuit detecting switching of at least one of said at least one variable gain amplifier*" is not clearly explained in the specifications, nor shown in the drawings. Furthermore, in paragraph

26 the applicant mentions that, "comparing circuit(s) may also serve as gain switching detection circuit(s)". However, the applicant doesn't clearly show how to make and/or use this feature.

For the purpose of art consideration on the merits, this limitation will be construed as being the comparison circuit. Furthermore, claim 3 will be objected to as failing to further limit the parent claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's prior art, and in view of Eliezer et al. (US Patent 6,735,260 B1), and

further in view of Mano et al, "Logic and Computer Design Fundamentals", 2nd edition, Published July 2000.

Re claim 1, applicant's prior art discloses a receiving apparatus comprising: at least one variable gain amplifier (See fig. 6: 305); at least one level detection circuit (See fig. 6: 306), which detects at least one level output from said at least one variable gain amplifier; at least one circuit for comparing at least one reference level to said at least one output from said at least one level detection circuit (See fig. 6: 314); at least one demodulator (See fig. 310 & paragraph 9); at least one binarizing circuit (See fig. 6: 312); at least one gain switching detection circuit detecting switching of at least one of said at least one variable gain amplifier (See fig. 6: 307, & paragraph 7)); wherein at least one gain of said at least one variable gain amplifier is switched based on at least one result of comparison by said at least one comparing circuit (See paragraph 7).

But the applicant's prior art fails to disclose at least one slice level holding circuit holding at least one substantially constant value at least one slice level employed by said at least one binarizing circuit; and at least one counter circuit; and wherein, when switching of said at least one gain is detected by said at least one gain switching detection circuit, said at least one counter circuit and said at least one slice level holding circuit causes said at least one slice level to be held at said at least one substantially constant value for at least one prescribed time. However, Eliezer et al does. (See Fig. 5: elements 72 & 86, & col. 9, line 67 through col. 10 line 1, & See Fig. 4: elements 42 &

44 & col. 10, lines 1-31. One skilled in the art would know that the holding will depend on the time constant set by the resistor and capacitor.)

Eliezer et al disclose an adaptive data slicer, which functions to adapt to changes in the properties of a signal input. It utilizes two peak detectors, a maximum peak detector and minimum peak detector. Furthermore, the peak detectors may be adapted to provide a hold input whereby an external processor can activate a holding mode in the data slicer. One skilled in the art would know that a processor may be programmed to act and operate as a counter. Subsequently, counters can be found inside a processor.

Therefore, taking the combined teachings of applicant's prior art and Eliezer et al as a whole, it would have been obvious to one of ordinary skill in the art to have incorporated these elements into the system of applicant's prior art, as taught by Eliezer, for the benefit of minimizing the bit error probability. (See abstract)

The combination of applicant's prior art and Eliezer et al fails to specifically disclose that a counter can be considered to be a processor. However, Mano et al does. (See chapter 5: pages 249-250)

Mano et al discloses that counters are sequential functional blocks, which are used extensively in the design of digital systems in general and digital computers in particular.

Therefore, taking the combined teachings of applicant's prior art, Eliezer et al, and Mano et al as a whole, it would have been obvious to one of ordinary skill in the art to have incorporated this feature in the manner as claimed, and as taught by Mano et al,

for the benefit of controlling or keeping track of the sequencing of activities in a digital system.

Re claim 2, the combination of Eliezer et al, and Mano et al, and the applicant's prior art further discloses that, wherein said at least one variable gain amplifier serves as at least one bandpass filter. (In applicant's prior art, see Fig. 6: element 305. One of ordinary skilled would know that a variable gain amplifier may also serve as a band-pass filter.)

Re claim 3, the combination of Eliezer et al, and Mano et al, and the applicant's prior art further discloses that, wherein said at least one comparing circuit serves as at least one gain switching detection circuit. (In applicant's prior art, see Fig. 6: element 307)

Re claim 4, the combination of Eliezer et al, and Mano et al, and the applicant's prior art further discloses that, wherein said at least one time counted by said at least one counter circuit is variable. (In Eliezer et al., see col. 9 line 67 through col. 10 line 1. The external processor can serve as a controlling for controlling, initiating, or triggering activities within a chip.)

Claim 5 has been analyzed and rejected w/r to claim 1. Furthermore, the processor can also control the demodulated signal holding circuit since this unit is

considered to be functional equivalent to the holding circuit disclosed by Eliezer et al.

Re claim 6, the combination of Eliezer et al, and Mano et al, and the applicant's prior art further discloses that, wherein said at least one binarizing circuit comprises: at least one offset canceler circuit outputting, when at least one signal input thereto is less than at least one lower cutoff value, said at least one signal corresponding to at least one amount by which said at least one input thereto is less than said at least one lower cutoff value, and outputting, when said at least one signal input thereto is greater than said at least one upper cutoff value, said at least one signal corresponding to said at least one amount by which said at least one of the signal input thereto is greater than said at least one upper cutoff value (In applicant's prior art, see paragraph 15); at least one integrating circuits integrating said at least one output therefrom; at least one offset canceler output holding circuit provided between said at least one offset canceler circuit and said at least one integrating circuit (In applicant's prior art, see fig. 8: element 504.); at least one adding circuit adding and feeding back at least one output from said at least one integrating circuit to at least one input signal (In applicant's prior art, see fig. 8: element 502.); and at least one sign determining circuit using the sign of at least one signal output from said at least one adding circuit to carry out binarization (In applicant's prior art, see fig. 8: element 505.); said at least one offset canceler output holding circuit functioning as said at least one slice level holding circuit. (In Eliezer et al., see col. 9, line 67 through col. 10 line 1. The processor can activate the holding mode. Furthermore, the processor can also control the offset canceler output holding circuit

since this unit is considered to be functional equivalent to the holding circuit disclosed by Eliezer et al.)

Claim 7 has been analyzed and rejected w/r to claim 6.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Flores whose telephone number is 571-270-1201. The examiner can normally be reached on Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LF
December 13, 2006

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER